Appl. No. 10/761,985
Examiner: Tran, Thien F, Art Unit 2811
In response to the Office Action dated May 19, 2005

Date: August 16, 2005
Attorney Docket No. 10113681

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently Amended): A dynamic random access memory cell layout, comprising:

a first ~~gate~~ conductor line pair and a second ~~gate~~ conductor line pair extending along a first direction, in which each conductor line pair comprises a first conductive line and a second conductive line, and in which each ~~gate conductor pair~~ conductive line comprises a ~~first~~ gate conductive line portion and a ~~second gate conductive~~ word line portion;

a bitline pair extending along a second direction and intersecting the ~~gate~~ conductor line pairs, in which the bitline pair comprises a first bitline and a second bitline;

a first active area extending along the second direction, crossing the first ~~gate~~ conductor line pair and corresponding to the first bitline; and

a second active area extending along the second direction, crossing the second ~~gate~~ conductor line pair and corresponding to the second bitline;

wherein, each active area comprises:

a first deep trench and a second deep trench formed in a substrate underneath the first ~~gate~~ conductive line and the second ~~gate~~ conductive line, respectively;

a bitline contact formed between the first ~~gate~~ conductive line and the second ~~gate~~ conductive line, in which the bitline contact is electrically connected to the corresponding bitline;

a common source/drain region formed in the substrate between the first ~~gate~~ conductive line and the second ~~gate~~ conductive line, in which the common source/drain region is electrically connected to the bitline contact;

a first vertical transistor formed overlying the first deep trench, in which the first vertical transistor comprises a first buried strap out-diffusion region formed in the substrate adjacent to one sidewall of the first deep trench; and

a second vertical transistor formed overlying the second deep trench, in which the second vertical transistor comprises a second buried strap out-diffusion region formed in the substrate adjacent to one sidewall of the second deep trench.

Claim 2 (Original): The dynamic random access memory cell layout as claimed in claim 1, wherein the first deep trench is partially overlapped with the first vertical transistor, and the sidewall profile of the first deep trench on the overlapping portion is a line shape.

Claim 3 (Original): The dynamic random access memory cell layout as claimed in claim 1, wherein the second deep trench is partially overlapped with the second vertical transistor, and the sidewall profile of the second deep trench on the overlapping portion is a line shape.

Claim 4 (Withdrawn): The dynamic random access memory cell layout as claimed in claim 1, wherein the first deep trench is partially overlapped with the first vertical transistor, and the sidewall profile of the first deep trench on the overlapping portion comprises at least three edges.

Claim 5 (Withdrawn): The dynamic random access memory cell layout as claimed in claim 4, wherein the sidewall of the first deep trench on the overlapping portion is a ⏃-shaped profile.

Claim 6 (Withdrawn): The dynamic random access memory cell layout as claimed in claim 1, wherein the second deep trench is partially overlapped with the second vertical transistor, and the sidewall profile of the second deep trench on the overlapping portion comprises at least three edges.

Claim 7 (Withdrawn): The dynamic random access memory cell layout as claimed in claim 6, wherein the sidewall of the second deep trench on the overlapping portion is a ⏃-shaped profile:

Claim 8 (Original): The dynamic random access memory cell layout as claimed in claim 1, further comprising a first deep trench capacitor formed at the lower portion of the first deep trench.

Claim 9 (Original): The dynamic random access memory cell layout as claimed in claim 1, further comprising a second deep trench capacitor formed at the lower portion of the second deep trench.

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Claim 10-18 (Canceled)